SUB-SAMPLING APPARATUS AND METHOD AND IMAGE SENSOR EMPLOYING THE SAME

Abstract of the Disclosure

The present disclosure relates to an address sub-sampling apparatus and method, and an image sensor employing the same. An address sub-sampling apparatus includes a counting unit that generates a binary address of N bits, N being a natural number larger than 2. The address sub-sampling apparatus also includes an address conversion unit that sub-samples the binary address of N bits to output a sub-sampled address having first, second and third bit groups, wherein the sub-sampled address is arranged in order of the third, the first and the second bit groups from the MSB (Most Significant Bit). The first bit group, which is a combination of digits in the sub-sampled address corresponding to the number of addresses to be skipped, being set as "0", the second bit group, which includes the LSB (Least Significant Bit) corresponding to bits of the binary address, and the third bit group, which includes the MSB being set to shift address subtracted by the number of bits in the first bit group from the MSB in the binary address.